A New Method for Specification of Parameters to Path Delay Faults Testing

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Abstract

Technology scaling and manufacturing process affect the performance of digital circuits, making them more vulnerable to environmental influences. Some defects are shown as delay faults therefore their testing is very important, mainly path delay faults. Such faults are tested over critical paths which have to be specified in a digital circuit. A problem of the critical paths selection is discussed in this paper. Some various factors have impact to signal propagation delay. A new method is presented for determining the measurement of the parameters impact on the path delay in the digital circuit. The method is focused to find the best weights of parameters for system PaCGen (Parameterized Critical Path Generator). The PaCGen is system for critical paths selection based on static timing analysis data with impact of factors to propagation delay. Accordingly, the critical paths are selected to be used for simulating fault coverage of path delay faults on transition delay fault model. Experimental results are provided using the ISCAS'89 benchmark circuits.

1.1 Introduction

Recent advances in development of new technologies have resulted in increasing complexity of the digital circuits and reducing their physical dimensions. Higher clock frequencies and technology scaling cause degradation of the digital circuits due to process variations and manufacturing defects.

Defects in digital circuits are modeled by the faults that are generally described as the inability to perform a function of the circuit defined in design specification. One of possible types of faults affecting performance of the digital circuits are delay faults which are reflected by changing specified timing parameter of the digital circuits. Several delay fault models exist and used in digital circuits testing from which a path delay fault model is more important based on its complexity.

The path delay fault represents the cumulative delay of a combinational path to exceed some specified duration. A combinational path begins at a primary input or a clocked flip-flop, contains a connected chain of gates, and ends at a primary output or a clocked flip-flop. A propagation delay is the time that a signal event takes to traverse the path [1]. The paths count in the circuit increases exponentially with its size. Therefore the path delay fault model is usually only used on a small portion of selected critical paths to generate test set for them. The critical paths are functional circuit paths with small timing slack necessary for the proper signal transition propagation [2]. The slack is a time margin (in picoseconds) which is left on a tested path for proper propagation of logical values transition.

The path delay is affected by a many factors. These factors may cause either speed up or slowdown of signal propagation in the circuit. Some parameters resulting directly from the physical implementation of the digital circuits, such as number of layers used, manufacturing technology or circuit aging, which allow the formation of secondary parameters such as power supply noise and voltage drop in certain

parts of the circuit or crosstalk effect between adjacent wires. The amount of the delay is also affected by ambient temperature and used delay faults testing method. In this case, there has to be taken into account parameters such as multiple inputs switching, signal transition type and test vectors used. All these parameters can affect the amount of the path delay alone or in a combination with each other.

The paper is organized as follows. The next section presents the factors and the third section describes a new method for specification of influence of these factors to path delay. Then they are parameters for criticality calculation of each path in a tested digital circuit. The fourth section describes experimental results over selected benchmark circuits. The paper is ended by conclusion with evaluation of the new method and possible future work.

1.2 Factors influencing the signal delay

Some existing and published factors with their impact to signal propagation delay were identified [3-11] and they are shortly described in this section.

A. Number of layers

Integrated circuits can be divided into two-dimensional (2D) and three-dimensional (3D). The 3D integrated circuits have been proposed as a solution to the growing delays on wires due to the technology scaling since the original manufacturing processes improved the speed of signal propagation. Connections between layers are realized with a through-silicon vias (TSV) filled with a conductive material. Incomplete filling of connections can cause an increased resistance on wire, thereby contributing to an increase in overall circuit delay. The final number of layers affects the amount of the delay, since each the TSV adds some delay to the signal propagation. The biggest difference in the amount of the delay occurs between the single-layer 2D and two-layer 3D circuit. With more layers, the amount of additional delay gradually decreases [3].

B. Aging

Aging is one of the most important reliability concerns in nanometer technology due to introducing a significant delay in the digital circuit over time, which may lead to its failure if the delay in the critical paths exceeds a timing constraints for which it was designed. One of the main causes of transistor aging is Bias Temperature Instability (BTI), which gradually increases a threshold voltage of the transistor, and thereby the circuit delay. The BTI-induced delay degradation rate of the transistor depends on several factors, such as the effects of process variations and workload and operating conditions that affect the temperature and voltage profile droop. Therefore, to accurately predict aging-induced the path delays, the effect of all these phenomena on circuit timing must be considered [4].

C. Power supply noise

Modern technology allows placing more transistors per chip and also increasing their operating frequency causing an increased current density and voltage drop along the supply networks. Power supply noise can be derived on the basis of inductive or resistive parameters or their combination. Inductive noise depends on the inductance and immediate current change, resistance noise is referred to as IR drop parameter and depends on current and distributed resistance in supply network. Another important factor is the components layout on a chip, in particular a location of switching gates, which creates different hot spots and the power supply noise levels around the critical path in every circuit [5].

D. Multiple input switching

This phenomenon arises when several logic gates inputs change their value in close time proximity. Static timing analysis (STA) assumes that logical value of an only one input is changed at a time while others maintain a stable value. This can cause problem when testing the delay faults. Multiple input switching can generate significant differences in the supply network, which are known as the power supply noise and with higher switching activity is the impact on the circuit delay much greater [6].

E. ***Crosstalk***

Due to continuous technology scaling, the distance between interconnecting wires is reduced, which allows to form a parasitic coupling capacitance between them causing crosstalk effects and impacting the circuit delay characteristics and performance [7]. Unfortunately, it is impossible to accurately analyze the crosstalk effects without test pattern information, because there is no way to count how many aggressors affecting the critical path delay with active coupling capacitance [2].

F. ***Temperature***

Chip temperature is affected by the dissipated power which depends on the thermal conductivity. Power dissipation hence leads to global temperature variations as well as local fluctuations in regions of high-activity. An increase in the temperature typically causes a circuit to slow down due to reduced carrier mobility and increased interconnect resistance [8]. However, this assumption fails for low voltage applications because the delay can decrease with increasing temperature values due to competitiveness between mobility and the supply voltage. This phenomenon is known as inverted temperature dependence [9].

G. ***Signal transition***

In older technology, logic gates were designed to have symmetrical rising and falling transitions, which led to larger cells and impaired the size of the design. Starting from 130nm technology, logic gates need not necessarily to observe this symmetry so rising or falling transition delay may be different, which can cause an additional delay [10].

H. ***Test vectors***

Test vectors used for detecting delay faults consist of a certain number of bits. This factor represent the number of undefined logical value in test vectors − X and $X \in (0,1)$. When test vectors have a large number of values X thus there is possible to apply test compression techniques. The compressed test can decrease the multiple input switching in dependence on logical values 0 and 1 assigned to X. The paths activated by such test vectors should produce less power consumption and test should be robust. By adjusting the values of bits containing undefined values can be achieved the reduction of impact to some other factors. The factors as multiple input switching, power supply noise effect and signal transition types can be adjusted by using the appropriate test vectors [11].

These factors have been selected for improving selection of critical paths in digital circuits in the context of the delay faults testing. The factors have been specified as parameters for criticality calculation of the paths in the digital circuits. Each parameter has different impact to the delays and therefore some weights for them have to be specified and involved in the expression of criticality calculation. The next section describes the new method for finding weights for the parameters in the expression shown also in the section.

1.3 A new method for weights specification of path delay parameters

Based on the analysis of the factors it can be concluded that the amount of additional delay caused by the influence of the multiple factors simultaneously is not equal to the sum of their individual delays. This is due to interdependencies between them, e.g. test vectors can increase the switching activity that leads to the higher power supply noise they are also occurred in higher temperature. All dependencies are shown in Figure 1. Arrows show the dependencies between factors. Start of the arrow show which factor has impact to other factor at the end of arrow. The range interval of impact to the signal propagation delay for each factor is also determined in Table 1. This values were derived from experimental results of published papers [3-11].

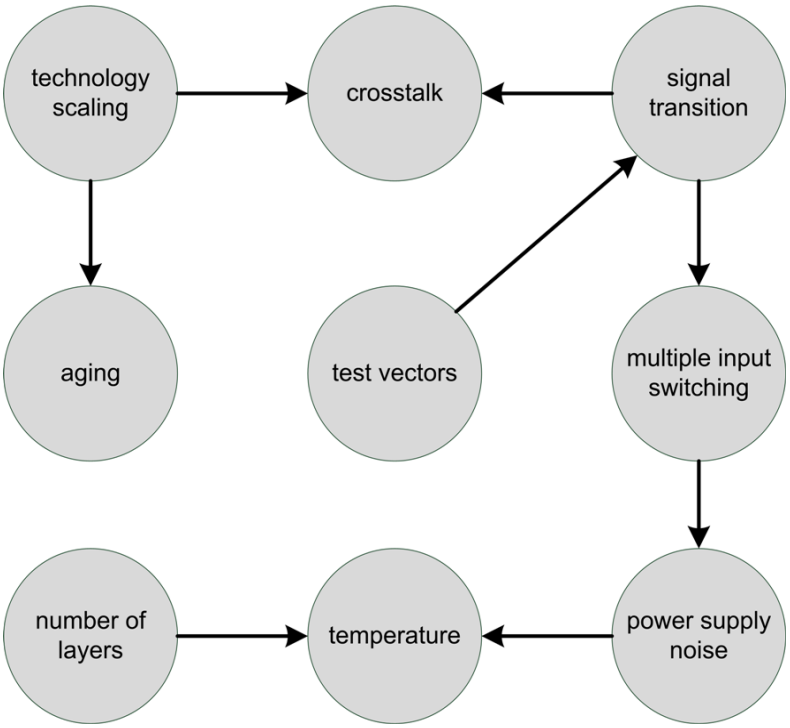

Figure 1. Dependencies between factors influencing the path delay

Table 1. Interval range for factors

Factor Name	Interval range [%]
Number of layers	3.4 - 7.2
Aging	8.0 - 13.5
Power supply noise	10.0 -19.0
Multiple input switching	8.7 - 18.2
Crosstalk	2.0 - 36.5
Temperature	3.0 - 5.0
Signal transition type	6.8 - 14.0
Test vectors	7.0 - 15.2

Generally, the critical paths can be specified by the static timing analysis (STA) or statistical static timing analysis (SSTA) and others. A new method has been proposed for selecting the critical paths based on path criticality calculation by system PaCGen [12]. In this method specification of influence of each factor is selected for a specific technology therefore it is necessary to develop a new method for estimation of the weights for these factors. Every path has a different kind of sensitivity to various factors and various technology that is described as a path weight. A list of critical paths for the tested circuit is generated from the STA information based on delays of individual paths and they are ordered by the delay size. For each critical path a new delay value is calculated using the following formula [12]:

$$c_p = \left(1 - \frac{S_p}{t}\right) \cdot \prod_{j=1}^{k} \left(1 - w_j\left(1 - i_{jp}\right)\right)$$

,

where:

c_p – criticality value of the path,

s_p – slack time of path from STA data,

t – time length of one clock period,

k – number of factors,

w_j – weight (impact) of parameter,

i_{jp} – calculated impact of parameter (sensitivity to the factor).

Recommended intervals of weights for individual factors are defined and included into the PaCGen system. The developed method is focused to find the best values for weight of PaCGen system parameters when delay fault coverage on transition delay fault model has maximal value. The resulting path delays are re-ordered according to the size of criticality. A set of critical paths is selected that is used to calculate the delay faults coverage in the digital circuit. Recommended range for weight values are presented in Table 2 for 45 nm and 90 nm CMOS technology. We calculate delay fault coverage of all possible combination of the weights at the recommended intervals with step 0.2 %. The recommended values of the parameters weight for specific technology is found when delay fault coverage has the maximal value.

Table 2. Recommended weight of parameters

Parameter	Recommended weight [%]
X-Filling	0.9 - 3.8
Power supply drop	1.4 - 4.8
Multiple input switching	0.5 - 4.5
Power consumption	0.2 - 0.7
Area overhead	0.5 - 1.0
Type of edge	0.4 - 2.8
3D	0.8 - 2.4
Sum	**4.7 - 20**

1.4 Experimental results

Experimental results were provided over selected ISCAS'89 benchmark circuits [13] with 45nm CMOS technology. The STA data were received from Cadence Encounter RTL Compiler. The delay fault coverage using the transition delay fault model was used for evaluation of the proposed method. The achieved results and improvements in comparison with the previous used method are presented in Table 3. The method has been implemented in the automatic system PaCGen [12]. First column of the table describes circuits and second one shows number of all paths in the circuits. Third column shows delay fault coverage from the system PaCGen when weights of parameters were used intuitively using values from Table 4. Fourth column presents delay fault coverage achieved by the proposed method when all possible combination of weights intervals from Table 2 were investigated. In all cases the same number of paths from all paths in the circuits was selected to demonstrate limited test length. This number was selected at 80 % of all existed paths in each circuit. Table 5 shows weights of parameters when maximum delay fault coverage was found. DC represents don't care value when this weight doesn't change delay fault coverage over all the interval from Table 2. Experiments are still in progress for other benchmark circuits and the results should be introduced during presentation.

Table 3. Delay fault coverage

Circuit	# all paths	Previous method [%]	Proposed method [%]	Improvement [%]
s27	56	73.8095	76.1905	2.3810
s298	462	71.5580	71.7391	0.1811
s382	800	65.2440	65.2440	0
s386	414	87.5358	87.6791	0.1433
s400	896	61.2637	61.4011	0.1374
s420	738	82.2917	82.5893	0.2976
s526	820	73.2033	73.7166	0.5133
s820	492	51.4049	51.4049	0
s953	462	33.6761	33.6761	0
s1488	192	24.9124	25.0875	0.1751

Table 4. Weights of parameters in previous method

Parameter	Weight [%]
X-Filling	3.8
Power supply drop	4.8
Multiple input switching	4.5
Power consumption	0.7
Area overhead	1.0
Type of edge	2.8
3D	2.4

Table 5. Weights with maximal delay fault coverage

Circuit	X-Filling [%]	PSD [%]	MIS [%]	Consumption [%]	Area [%]	Type of edge [%]	3D [%]
s382	<3.8	>2.6	>2.4	>0.4	<0.9	>2	DC
s420	1.8	5	4.4	0.8	DC	DC	DC
s526	1.8	2.6	2.4	0.4	0.5	2.6	1.2
s820	<3.8	DC	DC	DC	DC	<2.6	DC
s953	DC	>3.4	>3.4	DC	DC	DC	DC
s1488	DC	>3.4	>3.4	DC	DC	DC	DC

1.5 Conclusion

The paper presents the new method for specification of weights of some factors influenced delay in digital circuits. The issue of the proper estimation impact of various factors on the path delay in the digital circuits is a complex process due to the existing interdependencies between them, their dependencies on circuit structure and the fact that some of the factors may be changed over time. First

experiments over the selected benchmark circuits show that the presented method achieved slightly better results in delay fault coverage than the previous one. Future works will be aimed at improving the proposed method by setting the simulation more precisely to find more critical paths that may lead to more accurate results. This method will be also applied to other benchmark circuits for its effectiveness evaluation.

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