Survey of the Algorithms in the Column-Matching BIST Method

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Abstract

We propose a discussion on possible heuristic algorithms solving the major part of our BIST synthesis method – the Column Matching. The main part of our BIST design is an output decoder transforming pseudo-random LFSR code words into deterministic tests pre-computed by an ATPG tool. Synthesis of this decoder is based on coupling as many of its outputs with the inputs as possible, which significantly reduces its complexity. This NP-hard problem has to be solved by some heuristic algorithm.

1. Mixed-Mode BIST

The concept of a built-in self-test (BIST) became widely used in most of nowadays VLSI circuits, as their manufacture testing using only external ATE equipment is extremely time and memory demanding. Usually, the BIST structure consists of a pseudo-random test pattern generator (LFSR), followed by some additional logic modifying its code words somehow, to satisfy a better fault coverage. Many approaches were proposed before [1, 2]. To the most efficient techniques belongs a *mixed-mode* testing. Here pseudo-random patterns are applied to the circuit and then several deterministic tests are produced to cover the undetected faults. We have proposed a mixed-mode BIST design technique based on the column-matching principle [3, 4]. It is designed for a test-per-clock BIST for combinational or full-scan circuits. The main difference between our method and the others is that the test sequence is divided into two disjoint phases: the pseudo-random and the deterministic one. In the first phase the easy-to-detect faults are detected, and in the subsequent phase deterministic test vectors detecting the remaining faults are produced by a combinational *Decoder*. The *Switch* alternates between these two phases. Generally, it is an array of multiplexers.

The column-matching process consists of two linked NP problems. First, proper columns to be matched have to be selected. We have found that the best way is to do it at random. The second, more important problem is checking for the validity of the match. We have studied several heuristic methods and evaluated their efficiency. We have found a simple algorithm solving this problem efficiently in a short time.

2. Experimental Results

Here we present the results of the comparison with other methods, namely the bit-fixing [1] and row matching [2]. The *TL* columns indicate the test length, the *GEs* column the area overhead of the combinational circuit, in terms of the gate equivalents.

Table 3. Comparison results

	Col.-matching		Bit-fixing		Row-matching	
Bench	*TL*	*GEs*	*TL*	*GEs*	*TL*	*GEs*
c880	1 K	**10.5**	1 K	27	1 K	21
c1355	2 K	15	3 K	11	2 K	0
c1908	3 K	**7.5**	4 K	12	4.5 K	8
c2670	5 K	172	5 K	121	5 K	119
c3540	5.5 K	**1.5**	4.5 K	13	4.5 K	4
c7552	8 K	586	10 K	186	8 K	297
s420	1 K	**24.5**	1 K	28	-	-
s641	4 K	15	10 K	12	10 K	6
s713	5 K	16.5	-	-	5 K	4
s838	6 K	130	10 K	37	-	-
s1196	10 K	**6**	-	-	10 K	36

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