A new test-per-clock BIST method for combinational or full-scan circuits

**Main Idea**
If we reorder the \( C \) matrix and \( T \) matrix rows so that some \( C \) matrix and \( T \) matrix columns are equal, the outputs of the output decoder described by these columns will be implemented as mere wires.

Remaining outputs must be synthesized by some Boolean miniimzer (EESpresso: BOOM)

**THE COLUMN MATCHING ALGORITHM**

- Select one \( C \) matrix and one \( T \) matrix column randomly
- Try to match the columns

**DONE**

- Substitute don't cares
- Make test compaction
- Extract matched columns
- Minimize the remaining logic

**BLOCKING MATRIX**

- Binary matrix \( B \)
- \# of columns = \# of \( T \) matrix rows
- \# of rows = \# of \( C \) matrix rows
- \( B[i,j] = 1 \) when \( j \)-th \( C \) matrix row can be assigned to the \( j \)-th \( T \) matrix row
- \( B[i,j] = 0 \) otherwise
- After matching \( p \)-th \( C \) matrix column with \( q \)-th \( T \) matrix column \( B \) is modified:
  - \( B[i,j] \) is set to \( 0 \)

**Checking the correctness of a column match**

- For every \( B \) matrix column \( j \) find one different \( i \) so that \( B[i,j] = 1 \)
- Trivial task for test without don't cares
- \( NP \)-hard problem for a test with don't cares - similar to a CP solution

**EXAMPLE EXPERIMENTAL RESULTS**

-ISCAS BENCHMARKS
  - Test sets (with / without DCs) generated by ATOM tool
  - LFSR width = \# of benchmark inputs, 5000 code words
  - Quality of the result measured in gate equivalents

**CONCLUSIONS**

- New test-per-clock BIST method based on a design of a combinational block transforming LFSR code words into deterministic test patterns pre-generated by some ATPG tool was proposed

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