Minimization of Switching Activity of Graphene Based Circuits

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***Abstract*—Reduction of power dissipation is a key challenge of VLSI circuits designers. In traditional CMOS-based circuits, dynamic power dissipation occurs due to the switching activity, i.e., transitions at logic nodes. In graphene-based circuits, power dissipation is also caused by the switching activity. In this paper, we compute the switching activity of these circuits considering the switching at every transistor. We propose an algorithm to minimize the total switching activity of graphene-based logic circuits. The algorithm is tested on benchmark circuits and the results show the reduction of average switching activity, area, and switching activity $\times$ area respectively by 9.17%, 0.81%, and 9.82%.**

***Index Terms*—Graphene, Pass XNOR, Dynamic Power, Switching Activity.**

I. Introduction

Graphene has several advantageous electrical properties, such as high carrier mobility and saturation velocity [1]. But the absence of energy bandgap between the conduction and valency band of *Graphene* [2] prohibits the OFF state of a transistor made of graphene. Therefore, a graphene based CMOS transistor cannot be used as a digital device. Satisfactorily large energy gaps of very narrow *Graphene Nanoribbons (GNRs)* allow the use of the material as a semiconductor to implement Graphene-FETs [3]. But such *GNRs* suffer from edge roughness and edge disorder of the material, which results in the device characteristics degradation [4]. Equivalent graphene P-N junction [5] based on electrostatic doping can be used as a voltage-controlled passive register. Hence this type of P-N junction cannot be approved in modern silicon technology.

Pass-XNOR logic is an alternative logic style introduced in [6]. This pass-XNOR logic proficiently exploits the properties made available by graphene P-N junctions. Here a single P-N junction behaves as a transmission gate with embedded XNOR logic functionality. The series (parallel) connection of pass-XNOR gates implements AND (OR) logic. Feeding the second input of pass-XNOR gate to $0V$ implements the NOT gate. Thus, any Boolean logic function can be implemented with this gate.

In this paper, using two-input pass-XNOR logic gates, we implement the NOT gate and 2- and more-input AND, OR, NAND, NOR, XOR, and XNOR gates. Implementation of gates with more than two inputs by cascading two-input gates is also discussed. The total dynamic power consumption of these gates is due to the sum of two contributions: charging and discharging of input and load capacitances. The switching activity plays a major role in the dynamic power consumption. A traditional probabilistic method and the Parker and McCluskey method [7] can be used to compute the switching activity. The first method is exponential in nature and the second method consumes large memory. Hence, for large circuits these methods cannot be used. Using the signal probability based method, the switching activity can be easily computed. However, this method produces approximate results. In this paper we improve this method by optimizing the logic function at every node of a circuit. Using this method, the switching activity can be computed with better accuracy in linear time.

A set of transformation rules is proposed to minimize the switching activity. To the best of our knowledge, this is the first time discussion of estimation and reduction of switching activity of graphene based circuits.

The rest of the paper is organized as follows. Section II discusses the background of the Pass-XNOR Gate. Section III discusses the dynamic power modeling of the *graphene* P-N junction and calculation of the switching activity of *graphene*-based gates and circuits. A method to minimize the switching activity of graphene-based circuits is discussed in Section IV. Experimental results are presented in Section V. Finally, Section VI concludes the paper discussing the future scope.

II. Background

P-N junction based *graphene* circuits were introduced and discussed in [6], [8], [9]. A *graphene* P-N junction is constructed with a *graphene* sheet. The structure is shown in Fig. 1. Two metal-to-graphene contacts X and F on the top of the sheet act as the input and output respectively. The graphene sheet and two back-gates E and H are isolated by a thick layer of oxide. If the two back-gates E and H are supplied with the same voltage level (either "00" or "11"), then the two adjacent graphene regions will have the same doping profiles (either pp or nn) and hence all the carriers can pass through the junction. Hence it is an ON state [9]. On the other hand, if the two back-gates E and H are supplied with different voltage levels (either "01" or "10"), then the two adjacent graphene regions will have different doping profiles (either pn or np). Under this condition, the transmission probability ($T(\phi) = \cos^2(\phi)\exp^{-\pi K\delta\sin^2(\phi)}$ [5], here ϕ is the angle between the

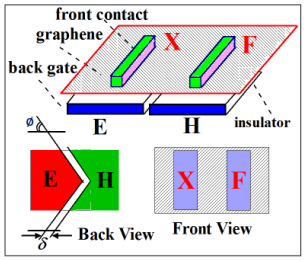


Fig. 1. Graphene P-N Junction [9]

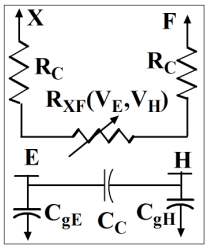
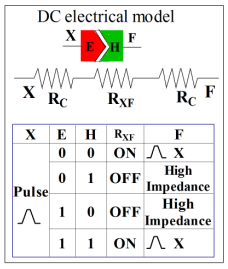


Fig. 2. Electrical Model of Graphene P-N Junction [9]

electron's wave vector k and the normal of the junction, δ is the metal pitch between the two split back gates and K is the Fermi momentum.) is very small. Hence it is practically an OFF state.



X	E	H	R_{XF}	F
Pulse	0	0	ON	X
	0	1	OFF	High Impedance
	1	0	OFF	High Impedance
	1	1	ON	X

Fig. 3. Functional behaviour of the pass-XNOR logic gates [9]

The electrical model of a P-N junction is shown in Fig. 2. Here, R_C (in the order of 10Ω) is the parasitic resistance of the metal-to-graphene contact. From the input (X) to the output (F), there is a resistive path with resistance R_{XF} and it is given by $R_{XF} = \frac{R_o}{NchT(\phi)}$. Here, R_o is the maximum resistance per propagation mode and N_{ch} is the number of excited propagation modes [10], [11]. R_{XF} can vary from $R_{ON} = 300\Omega$ to $R_{OFF} = 10^7\Omega$ [10]. At the 45nm (22nm) technology node, the lumped capacitance value C_g at the back-gates (i.e., CgE at E and C_{gH} at H) is approximately 302 aF (89 aF).

To implement the graphene gate, the logic level of X is high. When both E and H are supplied with the same voltage levels, then a conductive path is established from X to F. There is no conductive path if E and H are at different voltage levels. Hence this circuit behaves as an XNOR gate, considering E and H as inputs and F is the output [9]. This is shown in Fig. 3.

III. Dynamic Power Dissipation Model

The physics of *graphene* is similar to that of CMOS [12]. In $CMOS$ circuits, the power is dissipated mainly (about 80% of the total power) due to transitions between two logic levels – the switching activity. This kind of power dissipation is known as *dynamic power dissipation* [13]. Thus, the dynamic power and hence the total power consumption of VLSI circuits can be minimized by minimizing the switching activity. Calculation of the dynamic power consumption of a graphene P-N junction was described in [6], [8], [9]. We use the same calculation here. The dynamic power is consumed in a graphene P-N junction due to two stages. The charging/discharging of the input gate capacitance at the back-gates is the configuration phase and the corresponding power consumption is denoted by P_{conf}. The power consumed when charging/discharging the capacitive load at the front output is known as the evaluation phase and the corresponding power consumption is denoted by P_{eval}. Hence the total dynamic power dissipation is given by $P_{dynamic} = P_{conf} + P_{eval}$.

A pass-XNOR network can be converted into an equivalent resistor R_{eq} in series with the load capacitance C_l. Equivalent resistance R_{eq} can be calculated as a series/parallel connection of R_{ON} and R_{OFF}, depending on the back-gates configuration. Hence the instant power consumed across the resistor mesh can be calculated as $P_{eval} = R_{eq} i^2_{C_l}(t)$, where i_{C_l} is the current finally injected into C_l. The average value can be calculated as:

$$P_{eval} = \frac{1}{t_{rf}} \int_0^{t_{rf}} R_{eq} i^2_{C_l}(t) d(t) = \frac{R_{eq} C_l}{t^2_{rf}} C_l V^2_{dd} \quad (1)$$

Here, t_{rf} is the rise/fall output transition time and $i_{C_l}(t)$ is the current charging C_l [6], [8], [9]. Hence it is clear to see that when the number of transitions at the output of a node is increased, more dynamic power will be dissipated. Graphene shows power efficient performance if $t_{rf} > 10ps$ and the optimal value is $t_{rf} = \frac{1}{2.f}$ [14]. It reported in [10] that the total power at $10GHz$ and delay power product of graphene (CMOS) at $45nm$ technology node are respectively 5.59 ($5.78\mu W$) and 2.52 ($14.22\ ps.\mu W$).

A classical probabilistic approach of the switching activity calculation was given in [15]. Let the number of 1's and the number of 0's at an output node i in a circuit be given by $\mid \eta_i \mid$ and $\mid \chi_i \mid$, respectively. The probabilities of occurrence of 0 and 1, respectively, are given by the following equations:

$$P_0 = \frac{\mid \chi_i \mid}{\mid \eta_i \mid + \mid \chi_i \mid} \quad (2)$$

$$P_1 = \frac{\mid \eta_i \mid}{\mid \eta_i \mid + \mid \chi_i \mid} \quad (3)$$

Here we assume a uniform distribution of 0's and 1's at the primary inputs (PIs).

Definition 1. The switching activity of a node in a circuit is the probability of transition of logic state either from 0 to 1 or from 1 to 0 [16].

Hence at node i, the switching activity is given by

$$SA = P_0 \times P_1 = \frac{\mid \eta_i \mid \times \mid \chi_i \mid}{(\mid \eta_i \mid + \mid \chi_i \mid)^2} \quad (4)$$

In [16] a rule based method is proposed to reduce the switching activity of switching functions implemented in CMOS technology. In that paper, the switching activity is calculated and minimized at the gate level. In contrast to this, the switching activity is calculated at transistor level in this paper.

A. Graphene Gate and Switching Activity

Now we discuss some basic gates based on *graphene* pass transistor logic. From here onwards, by gate we mean a *graphene* gate. Fig. 4 shows the XNOR gate. In the output node of its truth table, the numbers of 0's and 1's are respectively 2 and 2. Hence $P_0 = P_1 = \frac{2}{4}$. Hence the switching activity is $\frac{2}{4} \times \frac{2}{4} = \frac{1}{4}$. Fig. 5 shows the NOT gate. If

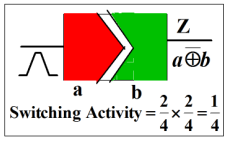


Fig. 4. Graphene XNOR

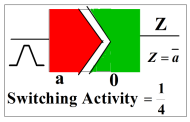


Fig. 5. Graphene NOT

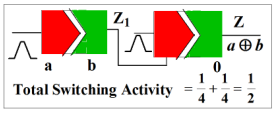


Fig. 6. Graphene XOR

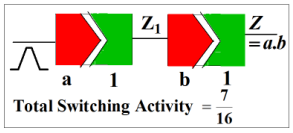


Fig. 7. Graphene AND

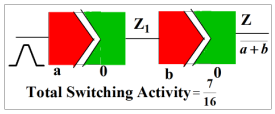


Fig. 8. Graphene NOR

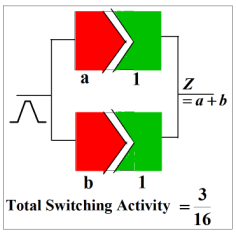


Fig. 9. Graphene OR

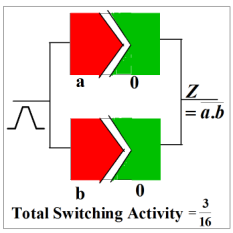


Fig. 10. Graphene NAND

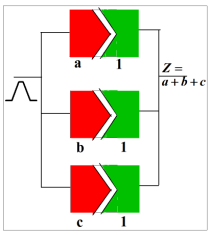


Fig. 11. Graphene 3 input OR

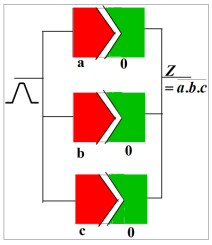


Fig. 12. 3-input NAND

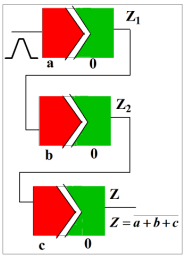


Fig. 13. 3-input NOR

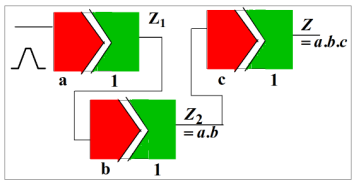


Fig. 14. 3-input AND

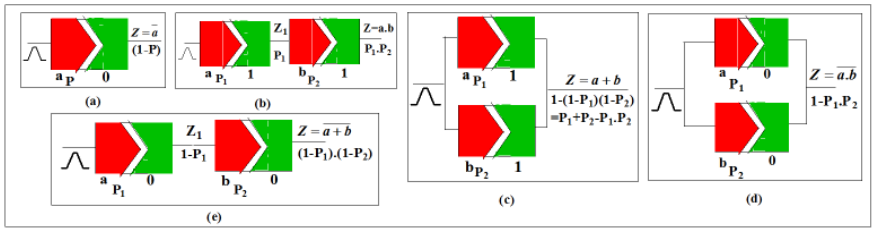


Fig. 15. Calculation of switching activity using signal probability

TABLE I
SWITCHING ACTIVITY OF GATES

Gate	No. of inputs	Switching Activity		
		Z1	Z2	Z(Total)
XOR	2	1/4	-	1/4+1/4=1/2
AND	2	1/4	-	1/4+3/16=7/16
	3	1/4	3/16	1/4+3/16+7/64=35/64
OR	2	-	-	3/16
	3	-	-	7/64
NAND	2	-	-	3/16
	3	-	-	7/64
NOR	2	1/4	-	1/4+3/16=7/16
	3	1/4	3/16	1/4+3/16+7/64=35/64

the supply voltage $a = 0$, then only the conductive path will be established since the other input is at logic 0. It is clear to see that the switching activity of this NOT gate is $\frac{1}{4}$. Figs. 6, 7, 8, 9, and 10 respectively show 2-input XOR, AND, NOR, OR, and NAND gates. Figs. 11, 12, 13, and 14 respectively show 3-input OR, NAND, NOR, and AND gates. Gates with four and more inputs can be implemented similarly. Switching activities of these gates are summarized in Table I.

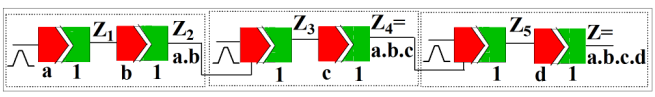


Fig. 16. Cascading AND Gates in a Chain Structure

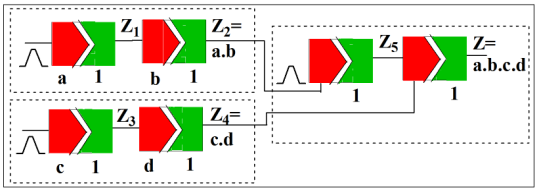


Fig. 17. Cascading AND Gates in a Tree Structure.

B. Calculation of Switching Activity Using Signal Probability

Using the signal probability, the switching activity can be easily computed. Fig. 15 shows the propagation of signal probabilities through gates. Table II shows the calculation of the switching activity using signal probability.

C. Effects of Switching Activity in Cascading of Gates

Now we discuss the cascading of two-input gates. Figs. 16 and 17 show the construction of 4-input AND gate by cascading two 2-input AND gates respectively by using the chain and tree structure. In the similar way OR and XOR gate can be cascaded. Table III shows the switching activities of these cascaded gates.

D. Calculation of Switching Activity of Logical Circuits

Now we discuss the calculation of switching activity of logic circuits. Consider a 4-variable function $f(a, b, c, d) = b\bar{c}d + \overline{bc} + \overline{a + d}$. Fig. 18 shows the corresponding circuit

TABLE II
SWITCHING ACTIVITY USING SIGNAL PROBABILITY

Gate	Input Probabilities		Probability at Z_1	Output Probability	Switching Activity
	Input 1	Input 2			
NOT	P	-	-	(1-P)	P(1-P)
AND	P_1	P_2	P_1	P_1P_2	$P_1(1-P_1)+P_1P_2(1-P_1P_2)$
OR	P_1	P_2	-	$1-(1-P_1)(1-P_2)$	$(1-P_1)(1-P_2)(1-(1-P_1)(1-P_2))$
NAND	P_1	P_2	-	$1-P_1P_2$	$P_1P_2(1-P_1P_2)$
NOR	P_1	P_2	$1-P_1$	$(1-P_1)(1-P_2)$	$P_1(1-P_1)+$ $(1-P_1)(1-P_2)(1-(1-P_1)(1-P_2))$

schematic. Here the switching activity is calculated considering the switching at each transistor. In Fig. 18, $Z_1 = \bar{c}$, $Z_3 = b\bar{c}$, Z_2 is the intermediate state of $Z_3 = b\bar{c}$. Similarly, $Z_4 = b\bar{c}d$, $Z_5 = \overline{bc}$, $Z_7 = \overline{a+d}$, $Z_8 = b\bar{c}d + \overline{bc} + \overline{a+d}$. Switching activity can be computed accurately by considering the truth tables of each and every node of a circuit. But this approach is a hard problem for circuits with a large number of primary inputs, as truth tables of all signals must be computed. The switching activity can also be computed exactly, by algebraic methods (Parker and McCluskey) as described in [7]. But this method is too memory-consuming. The exact total switching activity of the function $f(a, b, c, d)$ obtained by these two methods is $\frac{403}{256}$=1.574219.

In this paper we use signal probability based method for the computation of switching activity. This method produces approximate results. The switching activity of a particular node depends on switching activities of all the preceding nodes. Hence the signal probability based method does not ensure the accurate switching activity, due to reconvergent paths. Using this model, the switching activities of nodes Z_1 to Z_8 are respectively 0.25, 0.25, 0.1875, 0.109375, 0.1875, 0.25, 0.1875 and 0.022888. Hence the total switching activity is 1.44763. We further improve this method by optimizing the logic function at every node. The switching activity is computed with this optimized expression. This optimization will reduce the adverse effect due to reconvergent paths. Hence the error of computation will be reduced to some extent. In this method, at the time of computation of switching activity, the rules for optimization of logic functions are applied so that error of computation is minimized. Here, in this example, Z_8 is implemented with 3-input OR gate. But the optimized logic expression for the node Z_8 is $\overline{bc}+\overline{a+d}$. In this case the switching activity of node Z_8 is 0.152344 and hence the total switching activity is 1.574219. For this example, the exact switching activity is achieved. But in general we can achieve some approximate result very close to the exact one.

Consider another logic function $f_1 = AB + BC + CA$ and its implementation with two-input graphene gates. Here, the actual switching activity is $\frac{115}{64}$=1.796875. Now, $AB+BC$ and $AB+BC+CA$ can be optimized to $C(A+B)$ and $C(A+B)+CA$ respectively. Using the modified signal probability based method, the switching activity will be 1.795898. Although it is an approximate value, it is closer to the actual one.

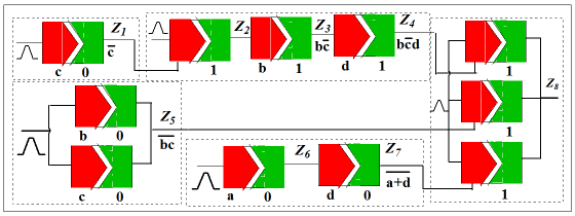


Fig. 18. Circuit schematic using GNR gate of $b\bar{c}d + \overline{bc} + \overline{a+d}$

IV. TRANSFORMATION OF EXPRESSION TO MINIMIZE THE TOTAL SWITCHING ACTIVITY

If a logical expression is transformed into a logically equivalent, but structurally different expression, the switching activity may be changed. Thus, a proper transformation of logical expression may reduce the switching activity. Here we measure the total switching activity at transistor level. The following rules and transformations of logical expressions will reduce the total switching activity of graphene based circuits. For CMOS based circuits, these rules were described in [16]. For all the rules described below, the total switching activity, delay, and area are calculated. For the NOT gate and 2-input XNOR, NAND gates, the delay is 1. The delay of 2-input AND, XOR and AND gates is 2. The area of a NOT gate and a 2-input XNOR gate is 1, whereas for 2-input AND, OR, XOR, XNOR, NAND and NOR gates, the area is 2. For 3-(4-) input AND, OR, NAND and NOR gates, the areas are 3 (4).

Rule 1 : For cascading AND/OR gates, use the chain structure instead of tree structure. But for cascading XOR gates, the tree structure sholud be preferred.

Rule 2 :

1) $X.Y + Y.Z = Y(X + Z)$. [$S.A._{LHS}$=$\frac{71}{64}$, $S.A._{RHS}$=$\frac{43}{64}$], [$\delta_{LHS} = 3$, $\delta_{RHS} = 3$] and [$A_{LHS} = 6$, $A_{RHS} = 4$].
2) $X_1Y_1 + X_2Y_1 + X_1Y_2 + X_2Y_2 + \ldots + X_1Y_n + X_2Y_n$ $=(X_1 + X_2)(Y_1 + Y_2 + \ldots + Y_n)$. [$S.A._{LHS}$=$\frac{14n}{16}$ + $\sum_{i=2}^{2n} \frac{2^i-1}{2^{2i}}$ Approx.,$S.A._{RHS}$=$\frac{10}{16}$ + $\sum_{i=2}^{n} \frac{2^i-1}{2^{2i}}$ Approx.], [$\delta_{LHS} = 2n + 1$, $\delta_{RHS} = n + 2$] and [$A_{LHS} = 6n - 2$, $A_{RHS} = 2n + 2$].
3) $X_1X_2 \ldots X_nY_1Y_2 \ldots Y_k + Y_1Y_2 \ldots Y_kZ_1Z_2 \ldots Z_p = Y_1Y_2 \ldots Y_k(X_1X_2 \ldots X_n + Z_1Z_2 \ldots Z_p)$. $S.A._{LHS}$=[$\frac{33}{16}$ + $\{\frac{(2^n-1)}{2^{2n}} + \sum_{i=2}^{(n-1)} \frac{(2^i-1)}{2^{2i}} \times 2\}$ + $\{\frac{(2^k-1)}{2^{2k}} + \sum_{i=2}^{(k-1)} \frac{(2^i-1)}{2^{2i}} \times 2\} \times 2$ + $\{\frac{(2^p-1)}{2^{2p}} + \sum_{i=2}^{(p-1)} \frac{(2^i-1)}{2^{2i}} \times 2\}$] and $S.A._{RHS}$=[$\frac{25}{16}$ + $\{\frac{(2^n-1)}{2^{2n}} + \sum_{i=2}^{(n-1)} \frac{(2^i-1)}{2^{2i}} \times 2\}$ + $\{\frac{(2^k-1)}{2^{2k}} + \sum_{i=2}^{(k-1)} \frac{(2^i-1)}{2^{2i}} \times 2\}$ + $\{\frac{(2^p-1)}{2^{2p}} + \sum_{i=2}^{(p-1)} \frac{(2^i-1)}{2^{2i}} \times 2\}$], [$\delta_{LHS} = 2(n+2k+p-2)$, $\delta_{RHS} = 2(n+p+k-3)+2$] and [$A_{LHS} = 2(n+2k+p-1)$, $A_{RHS} = (n+p+k-1)$].
4) $X_1X_2 \ldots X_nY_1Y_2 \ldots Y_m + Y_1Y_2 \ldots Y_kZ_1Z_2 \ldots Z_p = Y_1Y_2 \ldots Y_k(X_1X_2 \ldots X_nB_{k+1} \ldots B_m + Z_1Z_2 \ldots Z_p)$.

Rule 3 : Application of DeMorgan's theorem

TABLE III
SWITCHING ACTIVITY AND DELAY OF CASCADED GATES

Gate	No. of inputs	Chain Structure		Tree Structure	
		Switching Activity	Delay	Switching Activity	Delay
AND	4	$\frac{231}{256}$	6	$\frac{287}{256}$	4
	$n = 2^k$, $k \geq 1$	$\frac{1}{4}+\frac{(2^n-1)}{2^{2n}}+\sum_{i=2}^{(n-1)} \frac{(2^i-1)}{2^{2i}} \times 2$	$2 \times (n-1)$	$\sum_{i=1}^{(\lg_2^n)}(\frac{1}{4} + \frac{(2^{2i}-1)}{2^{4i}}) \times \frac{n}{2^i}$	$2 \times \lceil \lg_2^n \rceil$
	n (even) $\neq 2^k$, $k \geq 1$			$\sum_{i=1}^{(\lfloor \lg_2^n \rfloor)}(\frac{1}{4} + \frac{(2^{2i}-1)}{2^{4i}}) \times \lfloor \frac{n}{2^i} \rfloor$ $+(\frac{1}{4} + \frac{2^n-1}{2^{2n}})$	
	n (odd) $= 2m+1$, $m \geq 0$			$\sum_{i=1}^{(\lfloor \lg_2^n \rfloor)}(\frac{1}{4} + \frac{(2^{2i}-1)}{2^{4i}}) \times \lfloor \frac{m}{2^i} \rfloor$ $+(\frac{1}{4} + \frac{2^3-1}{2^6})$ $+(\frac{1}{4} + \frac{2^n-1}{2^{2n}})$	
OR	4	$\frac{91}{256}$	3	$\frac{111}{256}$	2
	$n = 2^k$, $k \geq 1$	$\sum_{i=2}^{n} \frac{2^i-1}{2^{2i}}$	$n-1$	$\sum_{i=1}^{(\lg_2^n)}(\frac{(2^{2i}-1)}{2^{4i}}) \times \frac{n}{2^i}$	$\lceil \lg_2^n \rceil$
	n (even) $\neq 2^k$, $k \geq 1$			$\sum_{i=1}^{(\lfloor \lg_2^n \rfloor)}(\frac{(2^{2i}-1)}{2^{4i}}) \times \lfloor \frac{n}{2^i} \rfloor$ $+(\frac{2^n-1}{2^{2n}})$	
	n (odd) $= 2m+1$, $m \geq 0$			$\sum_{i=1}^{(\lfloor \lg_2^n \rfloor)}(\frac{(2^{2i}-1)}{2^{4i}}) \times \lfloor \frac{m}{2^i} \rfloor$ $+(\frac{2^3-1}{2^6})$ $+(\frac{2^n-1}{2^{2n}})$	
XOR	4	$\frac{3}{2}$	6	$\frac{3}{2}$	4
	n	$\frac{1}{2}(n-1)$	$2 \times (n-1)$	$\frac{1}{2}(n-1)$	$2 \times \lceil \lg_2^n \rceil$

1) $\overline{X}+\overline{Y}$=$\overline{XY}$. [$S.A._{LHS}$=$\frac{11}{16}$, $S.A._{RHS}$=$\frac{3}{16}$], [$\delta_{LHS} = 2$, $\delta_{RHS} = 1$] and [$A_{LHS} = 4$, $A_{RHS} = 2$].
2) $\overline{X}.\overline{Y} = \overline{X+Y}$. [$S.A._{LHS}$=$\frac{15}{16}$, $S.A._{RHS}$=$\frac{7}{16}$], [$\delta_{LHS} = 3$, $\delta_{RHS} = 2$] and [$A_{LHS} = 4$, $A_{RHS} = 2$].

Rule 4: $XY + \overline{X}Z + YZ = XY + \overline{X}Z$(Consensus Theorem) [17]. [$S.A._{LHS}$=$\frac{33}{16}$ and $S.A._{RHS}$=$\frac{22}{16}$], [$\delta_{LHS} = 5$, $\delta_{RHS} = 4$] and [$A_{LHS} = 11$, $A_{RHS} = 7$].

Rule 5: $\overline{X}+XY = \overline{X+Y}+Y$. [$S.A._{LHS}$=$\frac{14}{16}$, $S.A._{RHS}$=$\frac{10}{16}$], [$\delta_{LHS} = 3$, $\delta_{RHS} = 3$] and [$A_{LHS} = 5$, $A_{RHS} = 4$].

Rule 6: $\overline{XY}$=$(\overline{XY})Y$. [$S.A._{LHS}$=$\frac{11}{16}$ and $S.A._{RHS}$=$\frac{9}{16}$], [$\delta_{LHS} = 3$, $\delta_{RHS} = 3$] and [$A_{LHS} = 3$, $A_{RHS} = 4$].

Rule 7: Application of Absorption Rules

1) $X\overline{Y} + Y$=$X + Y$ [17]. [$S.A._{LHS}$=$\frac{14}{16}$, $S.A._{RHS}$=$\frac{3}{16}$], [$\delta_{LHS} = 4$, $\delta_{RHS} = 1$] and [$A_{LHS} = 5$, $A_{RHS} = 2$].
2) $X\overline{Y} + \overline{Y}$=$\overline{XY}$(Modified Absorption Rule)[$S.A._{LHS}$=$\frac{18}{16}$, $S.A._{RHS}$=$\frac{3}{16}$], [$\delta_{LHS} = 4$, $\delta_{RHS} = 1$] and [$A_{LHS} = 5$, $A_{RHS} = 2$].
3) $\overline{X}Z + X\overline{Y}Z$=$Z(\overline{XY})$(Modified Absorption Rule) [$S.A._{LHS}$=$\frac{115}{64}$ and $S.A._{RHS}$=$\frac{39}{64}$], [$\delta_{LHS} = 6$, $\delta_{RHS} = 3$] and [$A_{LHS} = 10$, $A_{RHS} = 4$].

The switching activity reduces in all of the above transformations. Only for rule 6, the area from LHS to RHS is increased. For all other transformations, both the delay and area are either decreased or remain the same.

In order to reduce the switching activity of graphene based circuits, the logic expression of the corresponding circuits is expressed in terms of SOPs (POSs) first. Then the Algorithm shown in Fig. 19 is used to reduce the switching activity by applying the above rules to the logic expression.

Algorithm Minimize Switching Activity()

Input: Truth Table
Output: Function for minimal switching activity

Apply the standard logic optimization technique.
Apply Rule 1 and Rule 2 to reduce the switching activity.
if *no complemented literal* **then**
  Calculate the total switching activity.
end
if *number of complemented literals of is even* **then**
  apply De Morgan's theorem (Rule 3) on each pair of complemented literals.
end
if *applicable then* **then**
  Apply Rule 4, Rule 5, Rule 7 to reduce the switching activity.
end
if *a product term contains only one complemented literal* $\overline{x}_i$ **then**
  Apply Rule 6
end
if *the product term contains odd number of complemented literals* **then**
  First apply De Morgan's theorem (Rule 3) on each pair of complemented literals.
  Next apply rule Rule 6
end
Calculate the total switching activity

Fig. 19. Algorithm For Minimal Switching Activity

V. EXPERIMENTAL RESULTS

The experimental results are shown in Table IV. In this paper, we have synthesized several benchmark circuits from [18], [19], and [20] using conventional logic optimization methods. Optimization for area is used. Then, the proposed transformations are applied to these optimized circuits. The switching activities and areas of both results are computed and compared. The circuits are structurally optimized and mapped by ABC [21] using the following script iterated 20-times:

```
&get
&st; &synch2; &if -m -a -K 2; &mfs -W 10
&st; &dch; &if -m -a -K 2; &mfs -W 10
&put; map
```

The technology library used for the mapping reflected the real graphene gates sizes (see Section IV). We can observe that after applying the proposed transformations, the total switching activity is less or remains the same and the area

is also reduced in most of the cases and in the remaining few cases the area is equal or slightly worse. Fig. 20 shows the plot of switching activity $\times$ area before and after applying the transformations.

TABLE IV
COMPARISON OF SWITCHING ACTIVITIES OF DIFFERENT CIRCUITS

Circuit	Switching Activity (SA)		% Reduction of SA	Area		Area*SA	
	Before	After		Before	After	Before	After
cc[17]	13.78	11.33	17.78	121	117	1667.38	1325.61
lal[17]	13.78	13.13	04.72	111	111	1529.58	1457.43
ldd[17]	14.92	14.86	0.40	152	151	2267.84	2243.86
sct[17]	12.47	12.28	1.52	107	113	1334.29	1387.64
C17[18]	1.92	1.51	21.35	13	14	24.96	21.14
S27[19]	3.21	2.96	7.79	21	21	67.41	62.16
C432[18]	33.61	30.48	9.31	310	300	10419.10	9144.00
S499[19]	29.22	27.61	7.05	505	503	14756.10	13661.48
C499[18]	38.07	38.07	0	314	314	11953.98	11953.98
S3384[19]	15.84	13.09	17.36	102	94	1615.68	1230.46
C7552[19]	1.28	1.03	19.53	14	13	17.92	13.39
C5315[19]	246.16	238.24	3.22	2182	2171	537121.12	517219.04

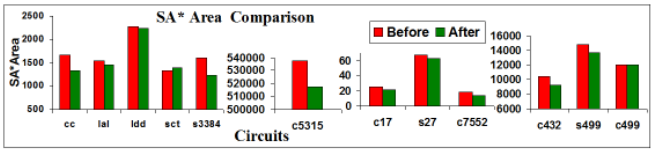


Fig. 20. Comparison of SA*Area

Following our algorithm the average reduction of switching activity is 9.17%, whereas the average reduction of area is 0.81%. In modern VLSI design, minimization of power dissipation is a key challenge. Hence reduction of the switching activity over other parameters is mostly favorable. The Switching Activity $\times$ Area product is reduced in most of the cases with the reduced switching activity. The average reduction of the Switching Activity $\times$ Area is 9.82%.

VI. CONCLUSION

In this paper, graphene-based implementations of basic gates and logic functions were discussed. We proposed a set of logic network transformations to reduce the switching activity of graphene based circuits. An improved signal probability based method was used to compute the switching activity. We observed that by applying the transformation rules, the switching activity and hence power dissipation of the circuits could be reduced. There are huge scopes of further improvement of this, specifically considering large circuits with exact computation of switching activity.

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