

Implicit Representations in Test Patterns Compression for Scan-Based Digital Circuits

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Abstract— Current test generation and compression processes still have a room for improvement. One important factor is the representation of test vector sets that a tool uses internally. We overview known approaches to this problem, and present our results obtained by using an implicit representation by instances of the satisfiability problem.

Keywords: Test compression, testing, implicit test representation

With the growing complexity of designs, the amount of test patterns needed to be stored and applied to the tested circuit grows up significantly. That is why the compression of test patterns is needed to decrease memory requirements and time consumption of the test.

ATPG (Automatic Test Pattern Generation) and compression of test patterns is based on manipulation of sets of binary vectors. The sets express the possibilities of choice (at least one vector from the set is needed) or summary (the whole set of vectors is needed). Such sets can be expressed *explicitly*, as an enumeration of vectors, or *implicitly*, by describing the required characteristic properties of the set.

The most frequently used formalism for implicit test characterization is the incompletely specified Boolean function. It cannot, however, describe *any* set of vectors. Therefore, while incompletely specified functions can improve the amount of data, the description remains partially explicit. Another function representations, like Binary Decision Diagrams (BDDs) [1] or And-Inverter Graphs (AIGs) [2] become of an interest to us. In these representations, the test set is described *implicitly*. The size of all these test representations grows exponentially with the circuit size.

A very popular implicit test patterns representation is a satisfiability problem (SAT) formulation. A SAT instance in CNF (Conjunctive Normal Form) is formulated for a given fault. Any satisfiable assignment of variables is a valid test pattern detecting this fault. In contrast to the previously mentioned representations, the CNF size grows linearly with the circuit size. For that reason, SAT-based ATPGs are becoming more and more popular.

Regarding the test pattern compression, there were several methods proposed. Many of these methods are based on using some encoding, like statistical codes [3, 4, 5, 6, 7], run-length codes [4, 5, 6, 8, 9], frequency directed codes (FDR) [8] and Golomb codes [10], others are based on XOR networks [11,

12], hybrid patterns [13], folding counters [14, 15], EDT (Embedded Deterministic Test) [16] and reuse of scan chains [17]. Another approaches are based on test pattern compaction [18, 19, 20] and overlapping [21, 22, 23, 24].

Our aim is to develop a better compression method for RESPIN [25] and similar decompression architectures. Compression is based on overlapping the test patterns in this case; therefore it requires choosing the right patterns in the right order to ensure optimum compression.

We have realized that the set of patterns detecting a fault can be naturally and compactly described by an instance of satisfiability problem (SAT) as it is done in SAT-based ATPGs [26, 27]. Furthermore, additional constraints can be easily added to the instance, selecting suitable patterns from the set.

Our tool, SAT Compress [28] uses such constraints to make sure that an overlap with previously generated data is possible. This allows us to generate only suitable vectors and generate them in the process of compression. The core algorithm is a simple greedy procedure, accepting the first vector that can be overlapped.

A comparison of compressed test lengths in bits for seven different state-of-the-art compression techniques and SAT-Compress are presented in Table I. Even with such a simple method we can obtain similar results such as these of the state-of-the-art compression methods and in some cases even better. The run time is longer, however, we are aware that test time and not test generation time is the bottleneck.

CONCLUSIONS AND FUTURE WORK

The test vectors representation influences substantially the architecture of test compression tools. The advantages of an implicit representation by SAT instances are documented on a compression tool for the RESPIN decompression architecture.

The existing algorithm and tool harness the basic benefits from the implicit characterization. However, generating, storing and handling the SAT instances can be much improved. The efficiency could then translate into a more thorough heuristic process, giving good results more consistently.

In farther view, RESPIN and the overlapping compression can be replaced with another decompressor, more compatible with the SAT description.

ACKNOWLEDGMENT

This research has been supported by MSMT under research program MSM6840770014 and by the grant of the Czech Grant Agency GA102/09/1668.

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TABLE I. COMPARISON OF THE TEST DATA SIZE FOR DIFFERENT COMPRESSION TECHNIQUES

Bench. circuits	MinTest [29]	Stat. Coding [7]	LFSR Reseeding [3]	Illinois Scan [30]	FDR Codes [8, 31]	EDT [16]	RESPIN++ [25]	COMPAS [21]	SAT-Compress
s5378	20,758	15,417	6,180	14,572	12,346	-	17,332	2,148	2,407
s9234	25,935	19,912	12,112	27,111	22,152	-	17,198	11,594	9,928
s13207	163,100	52,741	11,285	109,772	30,880	10,585	26,004	4,163	10,457
s15850	58,656	49,163	12,438	32,758	26,000	9,805	32,226	8,234	12,987
s35932	21,156	-	-	-	22,744	-	-	1,860	5,096
s38417	113,152	172,216	34,767	96,269	93,466	31,458	89,132	24,198	19,291
s38584	161,040	128,046	29,397	96,056	77,812	18,568	63,232	7,291	14,271