FAULT CLASSIFICATION FOR SELF-CHECKING CIRCUITS IMPLEMENTED IN FPGA

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Abstract. *This paper focuses on a fault classification problem for concurrent error detection circuits based on error detecting codes. The proposed fault classification differs from the common classification, where the faults are divided into two groups – the testable faults and the untestable faults. The faults are divided into four groups in our approach, by their impact to fault secure and self-testing properties. Our fault simulation software has been used to evaluate the proposed fault classification on real benchmarks. The benchmarks were implemented in a FPGA, and stuck-at-1 and stuck-at-0 fault model has been considered.*

1. Introduction

Nowadays when the circuit integration increases, the importance of radiation impact on integrated circuits grows. The FPGAs circuits are more sensitive to radiation than ASICs. Concurrent error detection (CED) techniques can allow faster detection of a soft error (error which can be corrected by reconfiguration process) caused by a Single Event Upset (SEU) [1][2]. SEU can also change values in the embedded memory used in the design. These changes are not detectable by off-line tests, but by some CED techniques only. There are three basic terms in a field of CED: fault security (FS), self-testing property (ST) and totally self-checking (TSC).

The use of ED codes and possibly some special synthesis methods need not ensure TSC property. It is necessary to evaluate how many faults violate the FS and ST property to make a comparison of different methods. In the common fault classification, the faults are divided into two groups according whether the faults are testable or not. But that classification is not sufficient for this purpose and new classification is needed.

A design technique for sequential circuits called MD-architecture (MD – Match detector) has been mentioned in [3]. Authors do not use an error detection code for the outputs, but they use specific properties of algorithmic state machines (ASM) for achieving the FS property. Another technique for self-checking (SC) sequential circuits is based on an

inverter-free design used together with codes that detect unidirectional errors such as Berger code or M-out-of-N code [4].

2. Proposed Fault Classification

The evaluation of error detection capabilities when the ED codes are used is more complicated. The correct output is not known during the processing. It is not sure that each fault causes an error and it is necessary to use a different approach to a fault classification. For each input vector, the reactions of a circuit in a presence of a fault can be divided into three groups:

- No error – the fault does not affect output values.
- Detectable error – the fault changes outputs into a noncode word.
- Undetectable error – the fault affects the outputs in such a manner, that the output vector is an incorrect codeword.

Every circuit has a set of allowed input vectors. These sets contain all possible vectors (2^n) for the combinational circuits. Sets for the sequential circuits are defined by circuit specification. The faults can be divided into four classes, among the circuit reaction on their presence. These classes are:

A) Faults that do not affect the output for any allowed input vector. Faults belonging to this class have no impact to the FS property, but if this fault can occur, a circuit cannot be ST.

B) Faults detectable by at least one input vector and for all the other input vectors they do not produce an incorrect codeword. These faults have no negative impact to the FS and ST property.

C) Faults that cause an incorrect codeword for at least one input vector and they are not detectable by any other input vector. Faults from this class cause undetectable errors. If any fault in the circuit belongs to this class, the circuit is neither FS nor ST.

D) Faults that cause an undetectable error for at least one vector and a detectable error for at least one another vector. Although these faults are detectable, they don't satisfy the FS property and so they are also undesirable.

With regard to the definitions of the FS and ST properties, we define these theorems:

- A circuit will be FS and ST only if all the faults belong to the class B.
- A circuit will be FS only if all the faults belong to the class A or B.
- A circuit will be ST only if all the faults belong to the class B or D.

These theorems follow directly from the definitions of FS and ST.

Most of the simulators (like FSIM [5] or HOPE [6]) compare the correct outputs with outputs in a presence of a fault. They cannot classify faults as precisely as we need. Due to this fact these simulators are not suitable. We had to use our own simulator.

3. Experimental Results

Our experiments are focused on the combinational and the sequential MCNC benchmarks [7]. The benchmarks were implemented in the Xilinx FPGA. Tables 2. – 5. contain the results of the experiments. These tables contain information about used circuits (first three columns). The next columns are: the number of all considered faults (All faults), the number of faults that cause a change at the outputs (X) for one input vector at least and the number of faults according to our classification (A, B, C, D) in Table 1.

3.1. Combinational circuits

The exhaustive test set generated for the combinational circuit is limited by the number of circuit's inputs. For circuits with more than 16 inputs the simulation time rapidly increases (doubles with every added input). Due to this restriction we use circuits with less than 16 inputs for our experiments only.

Two experiments have been done for combinational circuits, one with Hamming like codes (Table 2) and the second with the even parity (Table 3).

Table 2. Experiment 1 – combinational circuits and Hamming like code

Circuit	Inputs	Outputs	All faults	X	A	B	C	D
apla	10	17	1434	1409	25	1409	0	0
b11	8	37	736	734	2	734	0	0
br1	12	12	1014	994	20	972	0	22
al2	16	54	1180	1166	14	1166	0	0
alu2	10	12	1784	1784	0	1784	0	0

Table 3. Experiment 2 – combinational circuits and even parity

Circuit	Inputs	Outputs	All faults	X	A	B	C	D
apla	10	13	632	632	0	522	3	107
b11	8	32	418	416	2	321	42	53
br1	12	9	594	594	0	369	78	147
al2	16	48	628	627	1	576	17	34
alu2	10	9	830	819	11	757	0	62

The advantage of our classification is evident from the results of the experiment 2. Although more than 99% of all the faults change the output for one input vector at least (X), only 85% of all faults satisfy the FS property (A + B). About 96% of all faults satisfy the ST property (B + D).

3.2. Sequential circuits

In the experiments with sequential circuits, the state variables and outputs are coded by ED codes. The faults at the primary inputs are not considered. In the Experiment 3 we use an even parity code and in the Experiment 4 the M-out-of-N code (1 out of N for state variables and reduced M-out-of-N code for outputs). The results are shown in Table 4 and Table 5.

Table 4. Results of Experiment 3 – sequential circuits and even parity

Circuit	State bits	Outputs	All faults	X	A	B	C	D
s386	7	8	746	727	19	529	115	83
mark1	5	17	684	625	59	503	86	36
beecount	4	5	292	274	18	253	17	4
pma	6	9	1236	1131	105	826	99	206
ex6	4	9	670	645	25	407	143	95

Table 5. Results of Experiment 4 – sequential circuits and M-out-of-N code

Circuit	Sate bits	Outputs	All faults	X	A	B	C	D
s386	13	10	1018	988	30	943	45	0
mark1	15	18	678	649	29	616	33	0
beecount	7	4	306	296	10	275	17	4
pma	24	15	1214	1185	29	1146	17	22
ex6	8	14	790	760	30	725	24	11

Approximately 80% of all the faults (A+B) in the case of even parity and 95% in the case of M-out-of-N code satisfy the FS property. Approximately 82% of all faults in the case of even parity and 91% in the case of M-out-of-N code satisfy the ST property (B + D).

4. Conclusions and Future Work

This work supports the design process of CED circuits implemented in FPGAs. We propose a new fault classification. We can summarize that our classification leads to a more accurate evaluation of the fault coverage, and we can determine whether the tested circuit satisfies the FS and ST properties. We can also evaluate how many considered faults violate the FS and ST property. The classification allows us to distinguish which ED code is suitable for the chosen synthesis method with respect to the used fault model.

Our future work is devoted to evaluation of our solution for the structures [8] allowing to join small SC circuits into a large design as well.

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